REMARKS

The present Amendment amends claims 16 and 18, leaves claims 17 and 19 unchanged and cancels claims 14, 15, 20 and 21. Therefore, the present application has pending claims 16-19.

In paragraph 1 of the Office Action the Examiner alleges that claims 14, 15, 20 and 21 were withdrawn from further consideration being that they are directed to an invention that is independent or distinct from the invention originally claimed. Applicants do not agree. However, in order to expedite prosecution of the present application claims 14, 15, 20 and 21 were canceled. Applicants hereby reserve their rights to pursue the invention as set forth in claims 14, 15, 20 and 21 in a continuing/divisional application.

Claim 16 stands rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Particularly, the Examiner alleges that there is insufficient antecedent basis for the term "specification information". Amendments were made to claim 16 to clarify that the specification information is information input by the user for modifying the floorplan. This feature of the present invention corresponds to, for example, the specification information as illustrated in Fig. 19B of the present application and as discussed in the present application beginning on page 14 through page 17, line 9.

Therefore, sufficient antecedent basis exists for the phrase "specification information". Accordingly, reconsideration and withdrawal of the above described

rejection of claim 16 under 35 USC §112, second paragraph is respectfully requested.

Claims 18 and 19 stand rejected under 35 USC §102(e) as being anticipated by Barriientos (U.S. Patent No. 5,910,899); and claims 16 and 17 stand rejected under 35 USC §103(a) as being unpatentable over Ramachandran (U.S. Patent No. 6,002,857). These rejections are traversed for the following reasons. Applicants submit that the features of the present invention as recited in claims 16-19 are not taught or suggested by Barrientos or Ramachandran whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to claims 16-19 so as to more clearly describe features of the present invention. Particularly, amendments were made to claims 16-19 so as to more clearly describe that there are three types of information, circuit information of a module constituting a semiconductor integrated circuit, a floorplan which is a layout of blocks constituting the module, and evaluation indices which is generated based on the circuit information to be used for modifications of the floorplan. According to the present invention a module designer creates a module and a system LSI designer creates a floorplan of the module by combining blocks constituting the modules. Thus, according to the present invention the module designer creates the circuit information of the module and the evaluation indices while the LSI designer creates the floorplan. Thus, according to the present invention even if the module and LSI designers are different from each other it is

very important that the circuit information, the evaluation indices and the floorplan have corresponding relationships to one another to permit ease of use.

The present invention addresses the above by providing that the three sets information have corresponding relationships to each other and that, most particularly, the evaluation indices are generated based on the circuit information so as to be used for modifications of the floorplan.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by Barrientos or Ramachandran.

In the Office Action the Examiner alleges that Barrientos teaches Applicants evaluation indices. Applicants do not agree. The evaluation indices taught by Barrientos as well as the floorplan are generated by a floorplan tool maker. Thus, as per Barrientos the evaluation indices and the floorplan are created by the same designer.

In contrast, according to the present invention the module designer creates the evaluation indices as illustrated in Fig. 4A while a system LSI designer creates the floorplan as illustrated in Figs. 3A-3D. Thus, according to the present invention the floorplan and the evaluation indices are created based on the circuit information. This allows for correspondence relationships to be set forth in the information itself so that a user not having knowledge of designing such a circuit can easily modify the floorplan without deteriorating LSI performance. Such cannot be accomplished using Barrientos since the evaluation indices are not related in the database to the circuit information and as such are not within the general knowledge of a module designer but is, for example, within the general knowledge of a floorplan designer.

Thus, in Barrientos it would not be easy for one not having the general knowledge of a module or floorplan designing to modify or further configure the circuit so as to not effect efficiency. By use of the present invention such can be accomplished since the information contained therein is specifically related to each other so that modifications of one feature can be reflected as in effect in another feature.

Thus, Barrientos fails to teach or suggest an input unit for receiving, from external of an information processing system, circuit information of a module constituting a semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the modules, an evaluation indices, generated based on the circuit information of the module, for evaluating modifications of the floorplan as recited in the claims.

Therefore, it is quite clear that Barrientos does not anticipate nor render obvious the features of the present invention as now more clearly recited in the claims.

The above noted deficiencies of Barrientos are not supplied by Ramachandran, Therefore, combining the teachings of Barrientos with Ramachandran still fails to teach or suggest the features of the present invention as now recited in the claims.

In the Office Action the Examiner acknowledges that Barrientos did not specifically teach generating a plurality of floorplans and selecting one of the floorplans based on the evaluation result. The Examiner attempts to supply this deficiency by combining Barrientos with Ramachandran. The Examiner alleges that

Ramachandran teaches the generating of a plurality of floorplans and selection of one of the plurality of floorplans based on evaluation result.

However, Ramachandran does not supply the above noted deficiencies of Barrientos relative to the features of the present invention as now more clearly recited in the claims. Particularly, Ramachandran does not teach or suggest an input unit for receiving, from external of the information processing system, circuit information of a module constituting a semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module, and evaluation indices generated based on the circuit information of the module, for evaluating modification of the floorplan as recited in the claims.

Therefore, combining the teachings of Barrientos and Ramachandran still fails to teach or suggest the features of the present invention as now recited in the claims.

Accordingly, reconsideration and withdrawal of the above noted rejection of the claims based on a combination of Barrientos and Ramachandran is respectfully requested.

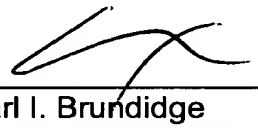
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 16-19.

In view of the foregoing amendments and remarks, Applicants submit that claims 16-19 are in condition for allowance. Accordingly, early allowance of claims 16-19 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.38174X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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